High-precision, Low-power Digital Temperature Sensor Compatible with SMBus and I²C Communications

1 Features

- Temperature range: −55°C to +125°C
- Temperature accuracy:
  ±0.5°C (−40°C to +125°C)
- Supply voltage range: 2.7V to 5.5V
- Low quiescent current：
  – Normal operation: ≤40μA
  – Shutdown mode: ≤0.3μA
- Resolution: 12bits, 0.0625 °C
- Digital output： compatible with SMBus™ and I2C interface
- Package: SOT23-6(2.92mm x 1.60mm)

2 Applications

- Power supply temperature monitoring
- Laptop
- Battery management
- Thermostatic control

3 Description

The GD30TS100N and GD30TS101N are two high-precision, low-power digital temperature sensors that can replace NTC/PTC thermistors and can be used for temperature measurement in communications, computers, consumer electronics, environment, industry, and instrumentation applications. The GD30TS100N and GD30TS101N can provide temperature accuracy of ≤ ±0.5°C within the normal operating range of −55°C to +125°C, and have good temperature linearity.

The rated operating voltage range of the GD30TS100N and GD30TS101N is 2.7V to 5.5V, and the quiescent operating current during temperature conversion is less than 40μA. The 12bit ADC integrated inside the chip has a resolution as low as 0.0625°C.

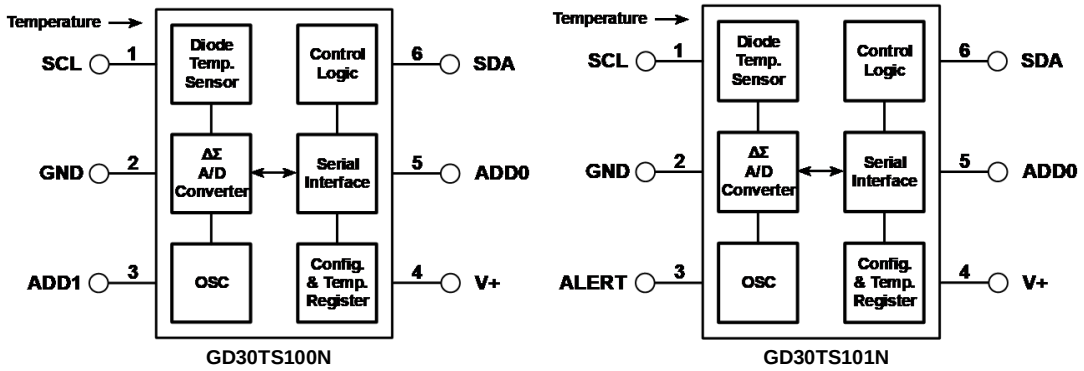
The GD30TS100N and GD30TS101N are available in the SOT23-6 package compatible with SMBus and I²C interfaces, and have the SMBus alarm function.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30TS100N	SOT23-6	2.92mm × 1.60mm
GD30TS101N		

1. For packaging details, see *Package Information* section.

Internal Schematic Diagram



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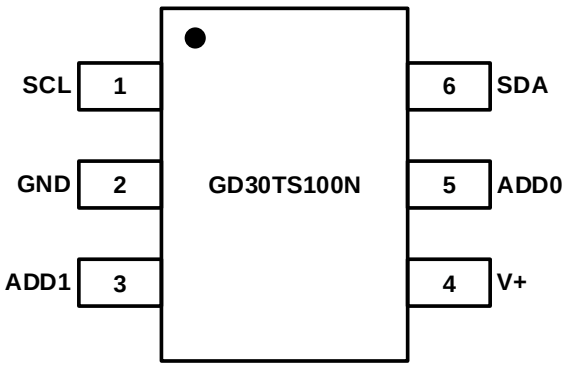
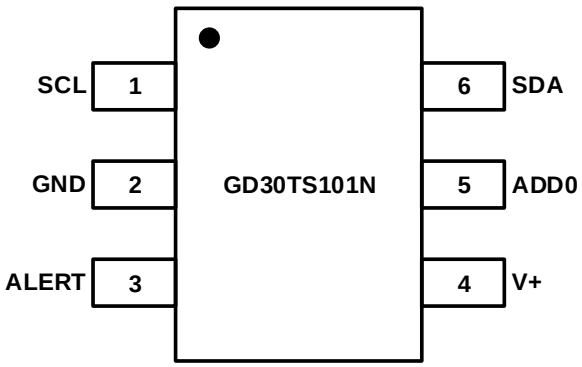
4.1 Pinout and Pin Assignment

SOT23-6
Top View



SOT23-6
Top View



4.2 Pin Description

PINS			PIN TYPE[1]	FUNCTION
NAME	GD30TS100N	GD30TS101N		
SCL	1	1	O	Serial clock. Open-drain output, requires a pull-up resistor.
GND	2	2	G	Ground.
ADD1	3		I	Address selects. Connected to V+, GND, or left floating.
ALERT		3	O	Over temperature alert. Open-drain output, requires a pull-up resistor.
V+	4	4	P	Supply voltage, 2.7V to 5.5V.
ADD0	5	5	I	Address selects. Connected to V+, GND, or left floating.
SDA	6	6	I/O	Serial data input. Open-drain output, requires a pull-up resistor.

1. P = power, G = Ground, I = input, O = Output, I/O=input/output.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_+	Power supply		6	V
V_{IO}	Voltage at SCL, SDA, and ADD0	−0.5	6	V
V_{ALERT}	Voltage at ALERT	−0.5	((V+)+0.3) and ≤ 5.5	V
T_J	Junction temperature		150	°C
T_A	Operating temperature	−55	125	°C
T_{stg}	Storage temperature	−60	150	°C

1. Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

5.2 Recommended Operation Conditions

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
V_+	Supply voltage	2.7	3.3	5.5	V
T_A	Operating Temperature	−55		125	°C

1. Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human Body Mode (HBM), per ANSI/ESDA/JEDEC JS-001	±5000	V
$V_{ESD(MM)}$	Machine Mode (MM), per JEDEC-STD Classification	300	V

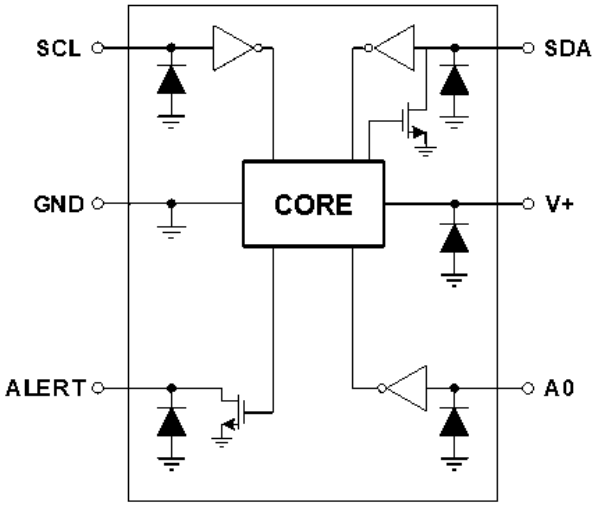


Figure 1. GD30TS101N Internal ESD Equivalent Circuit

5.4 Electrical Characteristics

Electrical characteristics of devices at T_A = +25°C and V+ = 2.7V to 5.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_A	Operating Temperature Range		−55		125	°C
T_{ERROR}	Accuracy (Temperature Error)	+25°C，V+ = 3.3V		±0.1	±0.5	°C
		0°C to +65°C, V+ = 3.3V		±0.25	±0.5	°C
		−40°C to +125°C		±0.5	±1	°C
	DC Power Supply Sensitivity	−40°C to +125°C		0.0625	±0.25	°C/V
	Resolution			0.0625		°C
				12		bits
	Temperature Measurement Resolution	R1 = 0, R0 = 0 (default)		9		bits
		R1 = 0, R0 = 1		10		
		R1 = 1, R0 = 0		11		
		R1 = 1, R0 = 1		12		
	Temperature Refresh Interval	R1 = 0, R0 = 0 (default)		40		ms
		R1 = 0, R0 = 1		80		
		R1 = 1, R0 = 0		160		
		R1 = 1, R0 = 1		320		
t_{TIME_OUT}	Timeout Time			30	40	ms
f_C	Bus Communication Frequency	Quick mode	0.001		0.4	MHz
		High-speed mode	0.001		2.5	
V_+	Power Supply Voltage		2.7	3.3	5.5	V
I_Q	Conversion Current	Bus free		40	75	μA
		Bus occupancy, SCL		70		
				150		
I_{SD}	Shutdown Current	Bus free		0.3	3	μA
		Bus occupancy, SCL		20		
				100		

6 Functional Description

6.1 Device Feature Description

6.1.1 Continuous Conversion Mode

The default working mode of the GD30TS100N and GD30TS101N is continuous conversion mode, and the typical conversion time is 26ms. During continuous conversion mode, the ADC performs continuous temperature conversions and stores each result to the temperature register, overwriting the result from the previous conversion. The conversion rate bits, R1 and R0, configure the GD30TS100N and GD30TS101N for conversion rates of 9bits, 10bits, 11bits or 12bits and adjust the temperature refresh interval accordingly. After each temperature measurement is completed, the chip will enter a low-power idle state (≤3μA) until the next temperature measurement begins. The duration of the idle state is determined by R1 and R0. The above process is shown in Figure 2.

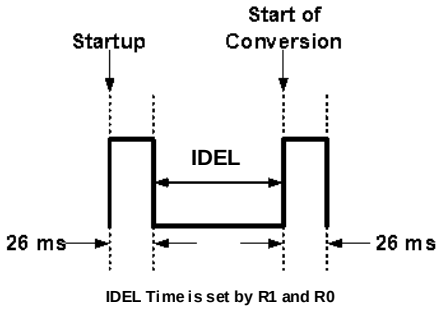


Figure 2. Schematic Diagram of Continuous Conversion

The temperature measurement range of the GD30TS100N and GD30TS101N is −55°C to +125°C. The read-only temperature register in GD30TS100N and GD30TS101N uses two bytes to store the temperature measurement results, as shown in Table 1. Byte 1 is the MSB, byte 2 is the LSB, the high 12 bits are used to indicate the temperature, and the remaining low bits are 0. When R1 and R0 configure the temperature measurement resolution to 9 bits, 10 bits or 11 bits, the high 9, 10 and 11 bits of the temperature register are used to store the temperature measurement results, and the remaining low bits are 0.

Table 1. 12-bit Temperature Data Format in Normal Temperature Measurement Mode

TEMPERATURE (°C)	DIGITAL OUPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
−0.25	1111 1111 1100	FFC
−25	1110 0111 0000	E70
−55	1100 1001 0000	C90

The temperature registers of the GD30TS100N and GD30TS101N use the binary complement form to represent the negative temperature results. When powered on or reset, the temperature registers of the GD30TS100N and GD30TS101N will be set to 00h until the next temperature conversion is complete.

6.1.2 Shutdown Mode

The shutdown mode of the GD30TS100N and GD30TS101N device allows the user to conserve power by shutting down all device circuitry except the serial interface, thereby reducing the current of the GD30TS100N and GD30TS101N to less than 0.3μA. The shutdown mode is initiated when the SD bit in the configuration register is set to 1; after configuring the registers in this way, the GD30TS100N and GD30TS101N will shut down after completing the current conversion. To exit the shutdown mode, write SD bit to 0, the GD30TS100N and GD30TS101N will re-enter continuous conversion mode.

6.1.3 One-Shot Mode

The GD30TS100N and GD30TS101N can be configured in the One-Shot mode. When the GD30TS100N and GD30TS101N are in the shutdown mode, writing 1 to the OS/ALERT bit in the configuration register starts a single temperature conversion. The GD30TS100N and GD30TS101N feature a one-shot mode. When the GD30TS100N and GD30TS101N are in the shutdown mode, writing 1 to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads 0. The GD30TS100N and GD30TS101N return to the shutdown state at the completion of the single conversion, the OS bit reads 1. When continuous temperature measurement is not required, this function can significantly reduce chip power consumption.

6.1.4 Alarm Function (ALERT)

The GD30TS100N and GD30TS101N have a temperature alarm function, by writing the TM bit in the configuration register as 0 or 1, the GD30TS100N and GD30TS101N can be configured as the comparator mode or the interrupt mode to achieve different alarm functions.

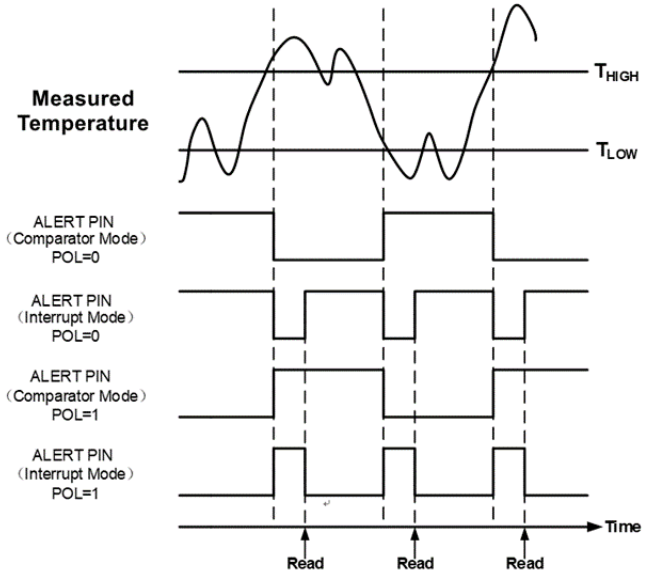


Figure 3. Status of the ALERT Pin in Different Modes

In the comparison mode (TM=0), when the number of times the temperature measurement result continuously equals or exceeds the temperature upper limit register value T_{HIGH} reaches the value defined by the F1/F0 bits in

the configuration register (as shown in Table 2), the ALERT pin will be activated. The ALERT pin will remain active until the number of times the temperature measurement result is continuously lower than the temperature lower limit register value T_{LOW} reaches the value defined by F1/F0.

In the interrupt mode (TM=1), the ALERT pin will be activated when the temperature measurement result equals or exceeds T_{HIGH} continuously for a number of times to the value defined by F1/F0 (as shown in Table 2). The ALERT pin remains active until it is cleared by one of three events: a read of any register, a successful SMBus alert response, or a shutdown command. After the ALERT pin is cleared, the device starts to compare temperature readings with the T_{LOW}. The ALERT pin becomes active again only when the temperature drops below T_{LOW} for a consecutive number of conversions as set by F1/F0 bits. The ALERT pin remains active until cleared by any of the same three clearing events. The user can also reset the GD30TS100N and GD30TS101N to clear the ALERT pin state by using the global response reset command (General Call). This operation also resets other internal registers in the GD30TS100N and GD30TS101N and returns the device to compare mode (TM=0). Table 2 shows the specific configuration of the F1/F0 bits.

Table 2. Number of Over-temperature Required to Activate the ALERT Pin

F1	F0	REQUIRED NUMBER (TIMES)
0	0	1 time (Default)
0	1	2 times
1	0	4 times
1	1	6 times

The polarity bit (POL) in the configuration register allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high. The above situations are shown in Figure 3.

The OS/ALERT bit in the configuration register can also display the alarm status of the chip in the comparison mode. When POL=0, when the number of times the temperature measurement result continuously equals or exceeds the temperature upper limit register value T_{HIGH} reaches the value defined by the F1/F0 bits in the configuration register, the OS/ALERT bit will change from 1 to 0; when the number of times the temperature measurement result continuously equals or exceeds the temperature upper limit register value T_{HIGH} reaches the value defined by the F1/F0 bits in the configuration register, the OS/ALERT bit will change from 0 to 1. When POL=1, the value of the OS/ALERT bit in the above process will be inverted.

The OS/ALERT bit is not affected by the TM bit. The OS/ALERT bit is 0 when powered on or reset, and will be set to 1 immediately by the above function.

6.2 Serial Interface

6.2.1 Bus Overview

The GD30TS100N and GD30TS101N is compatible with SMBus and I^2C interfaces. In the SUMBus protocol, the device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high-to low-logic level when the SCL pin is high. All slaves on the bus receive the 8-bits slave address on the rising edge of the clock, and the last bit indicates whether a read or write operation

is intended. During the ninth clock pulse, the addressed slave generates an acknowledge and pulls the SDA pin low to respond to the master. A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. When all data are transferred, the master generate a STOP signal to end the communication by pulling SDA from low to high when SCL is high.

During the data transfer, the SDA pin must remain stable when the SCL pin is high because any change in the SDA pin when the SCL pin is high is interpreted as a START or STOP signal.

6.2.2 Serial Bus Address

To communicate with the GD30TS100N and GD30TS101N, the master must first address slave devices through an address byte. The address byte has seven address bits and a read-write (R/W) bit that indicates the intent of executing a read or write operation. The GD30TS100N has two address pins, which can generate up to 8 different slave addresses; The GD30TS101N has one address pin, which can generate up to 3 different slave addresses. By connecting the address pins to V+, GND or floating, the host can address up to 8 GD30TS100Ns with different addresses or 3 GD30TS101Ns with 3 different addresses on a single bus. Table 3 and Table 4 give the connection method of the ADD0 pin corresponding to each slave address.

Table 3. Address Pin and Slave Addresses in GD30TS100N

ADD1	ADD0	SLAVE ADDRESS
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111

Table 4. Address Pin and Slave Addresses in GD30TS101N

ADD0	SLAVE ADDRESS
0	1001000
Float	1001001
0	1001010

6.2.3 Writing and Reading Operation

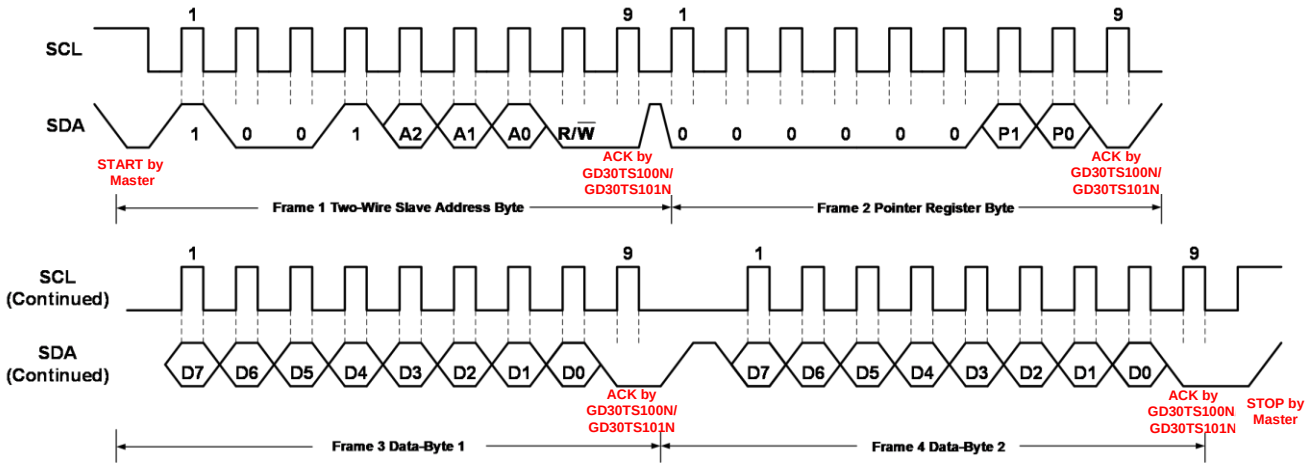


Figure 4. Two-wire Write Command Timing Diagram

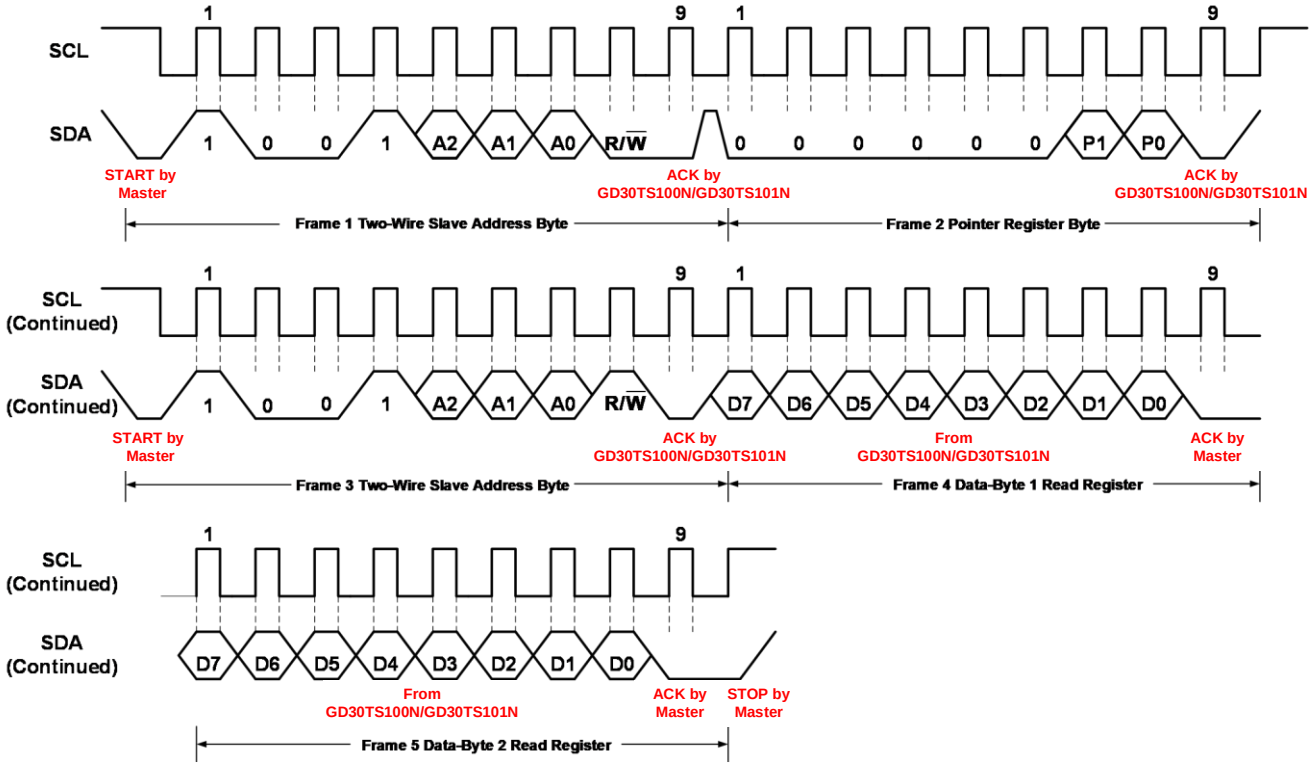


Figure 5. Two-wire Read Command Timing Diagram

When writing data to the GD30TS100N and GD30TS101N, after the slave address byte is sent, accessing a particular register on the GD30TS100N and GD30TS101N is accomplished by writing the appropriate value to the pointer register. Every write operation to the GD30TS100N and GD30TS101N requires a value for the pointer register.

When reading from the GD30TS100N and GD30TS101N device, after the slave address byte is sent, the corresponding pointer register byte also needs to be sent. Unlike the write operation, if the user needs to repeatedly read data from the same register, it is not required to send the pointer register byte separately each

time, the last value stored in the pointer register will be read by the device automatically; to change the register pointer for a read operation, a new value must be written to the pointer register. The action is accomplished by issuing a slave-address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command.

It should be noted that register bytes are sent with the MSB first, followed by the LSB. Figure 4 and Figure 5 show schematic diagrams of the above read and write operations.

6.2.4 SMBus Alert Function

The GD30TS100N and GD30TS101N support the SMBus alert function. When the GD30TS100N and GD30TS101N operate in interrupt mode (TM=1), the master can send out and SMBus ALERT command (19h) to the bus. If the ALERT pin is active, the device acknowledges the SMBus ALERT command and responds by returning the slave address. The eighth bit (LSB) of the slave address byte indicates if the alert condition is caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. This bit is equal to POL if the temperature is greater than or equal to T_{HIGH}; this bit is equal to POL if the temperature is less than T_{LOW}.

If multiple devices on the bus respond to the SMBus ALERT command, the bus will return the lowest two-wire address. The GD30TS100N and GD30TS101N ALERT pin becomes inactive at the completion of the SMBus ALERT command; the ALERT pin of the GD30TS100N and GD30TS101N that does not return an address will remain active. Sending the SMBus ALERT command again can continue to clear the ALERT pin of the GD30TS100N and GD30TS101N with the current lowest address. The above process is detailed in Figure 6.

The GD30TS100N acts the same as the GD30TS101N after sending the SMBus alarm command. The ALERT pins cannot be cleared without the ALERT pins, but can still return the slave address that activates the alarm.

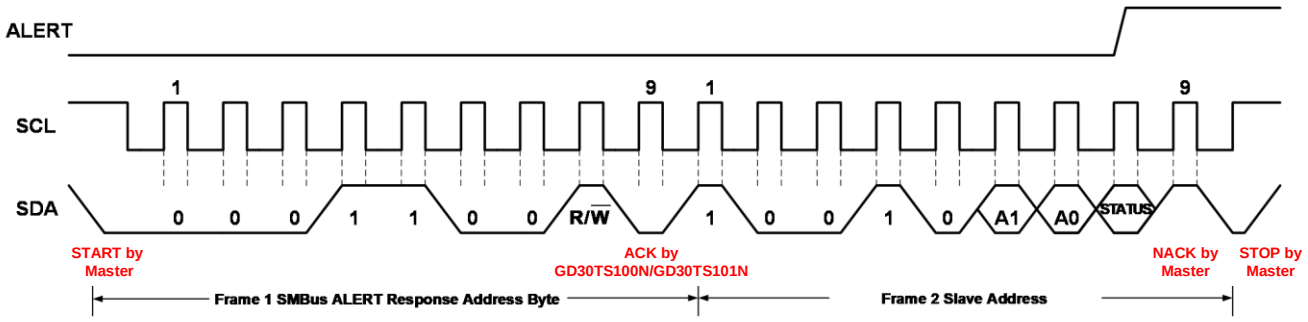


Figure 6. SMBus Alert Timing Diagram

6.2.5 General Call Reset

The GD30TS100N and GD30TS101N responds to the two-wire general call address 00h. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 06h, the GD30TS100N and GD30TS101N reset the internal registers to the power-up reset values, and aborts the current temperature conversion. If the second byte is other value, the GD30TS100N and GD30TS101N will not respond.

6.2.6 High-Speed Mode

For the two-wire bus to operate at frequencies above 400kHz, the host device must issue a High-Speed mode host code (00001xxxb) as the first byte after a START condition to switch the bus to high-speed operation. The

GD30TS100N and GD30TS101N device does not acknowledge this byte, but it does switch the input filters on the SDA and SCL and the output filters on the SDA to operate in High-Speed mode, allowing the bus to transmit data at frequencies up to 2.75MHz. After the High-Speed mode host code is issued, the host transmits a two-wire device address to initiate a data transfer operation. The bus continues to operate in High-Speed mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the GD30TS100N and GD30TS101N switches the input and output filters back to fast-mode operation.

6.2.7 Time-Out Function

The GD30TS100N and GD30TS101N resets the serial interface if SCL is held low for 30ms (typical) between a START and STOP condition, the GD30TS100N and GD30TS101N releases the SDA bus and waits for a START condition. To avoid activating the Time-Out function, a communication speed of at least 1kHz must be maintained.

6.3 Register Descriptions

6.3.1 Pointer Register

Figure 7 shows the internal register structure of the GD30TS100N and GD30TS101N device. The 8-bit Pointer Register of the device is used to address a given data register. The Pointer Register uses the two LSBs (see Table 5) to identify which of the data registers must respond to a read or write command. The power-up reset value of P1/P0 is '00'. By default, the GD30TS100N and GD30TS101N read the temperature on power-up.

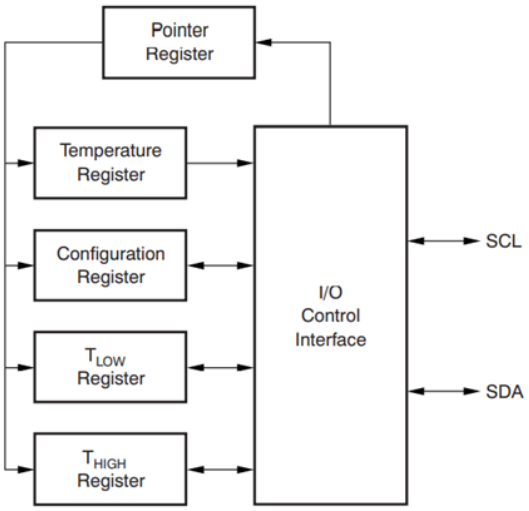


Figure 7. Internal Register Structure

Table 5 lists the pointer address of the registers available in the GD30TS100N and GD30TS101N device. During a write command, bytes P2 through P7 must always be 0.

Table 5. Pointer Address

P1	P0	REGISTER
0	0	Temperature Register (Read Only)
0	1	Configuration Register (Read/Write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

Table 6. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

6.3.2 Temperature Register

The Temperature Register of the GD30TS100N and GD30TS101N device is configured as a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 7. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The T11~T0 bits (T12~T0 bits in extended mode) are used to indicate temperature.

Table 7. Data Format of Temperature Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	T11	T10	T9	T8	T7	T6	T5	T4
2	T3	T2	T1	T0	0	0	0	0

6.3.3 Temperature Limit Register

The temperature limits are stored in the T_{HIGH} and T_{LOW} registers in the same format as the temperature result. Table 8 and Table 9 list the format for the T_{HIGH} and T_{LOW} registers. When the temperature measurement resolution of the chip is 9~11 bits, the 12bits data of the THIGH and TLOW registers also participate in the temperature comparison of the alarm function. The power-on reset values of the T_{HIGH} and T_{LOW} registers are:

T_{HIGH} = +80°C； T_{LOW} = +75°C.

Table 8. Byte 1 and 2 of T_{HIGH} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
2	H3	H2	H1	H0	0	0	0	0

Table 9. Byte 1 and 2 of T_{LOW} Register

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
2	L3	L2	L1	L 0	0	0	0	0

6.3.4 Configuration Register

The Configuration Register of the GD30TS100N and GD30TS101N is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Table 10 list the format and power-up and reset values of the configuration register.

Table 10. Configuration Register High Byte

BIT	FIELD	DEFAULT	DESCRIPTION
7	OS /ALERT (R)	1	**One-Shot and Interrupt Mode Alarm Flag Bit**
6	R1 (R/W)	0	**Temperature Measurement Resolution Flag** **00** = 9 bits, 0.5℃ **01** = 10 bits, 0.25℃ **10** = 11 bits, 0.125℃ **11** = 12 bits, 0.0625℃
5	R0 (R/W)	0	
4	F1 (R/W)	0	**The Number of Over-temperature Flags Required to Activate the ALERT Pin** **00** = 1 time **01** = 2 times **10** = 4 times **11** = 6 times
3	F0 (R/W)	0	
2	POL (R/W)	0	**ALERT Pin Polarity Flag** **1** = ALERT pin is high when activated **0** = ALERT pin is low when activated
1	TM (R/W)	0	**Chip Working Mode Flag under ALERT Function** **1** = Interrupt mode **0** = Comparator mode
0	SD (R/W)	0	**Shutdown Mode Flag** **1** = Shutdown mode **0** = Continuous conversion mode

7 Application Information

The above contents are the precautions for the GD30TS100N and GD30TS101N recommended by GigaDevice in practical applications. Customers are responsible for determining suitability of components for their purposes based on their own usage needs and application scenarios. Customers should test and verify their design implementation to confirm system functionality and avoid losses.

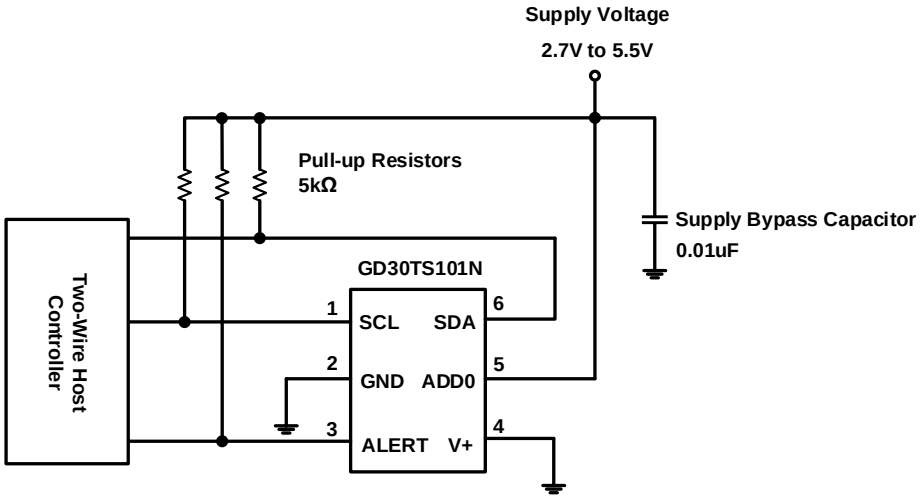


Figure 8. Typical Connections of the GD30TS101N

The GD30TS100N and GD30TS101N device requires pull-up resistors on the SCL, SDA, and ALERT pins, as shown in Figure 8, the recommended value for the pull-up resistors is 5kΩ. In some applications the pull-up resistor can be lower or higher than 5kΩ but must not exceed 3mA of current on any of those pins.

The GD30TS100N and GD30TS101N device is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V+ pin of the GD30TS100N and GD30TS101N device can further reduce any noise that the device might propagate to other components. R_F in Figure 9 must be less than 5kΩ and C_F must be greater than 10nF.

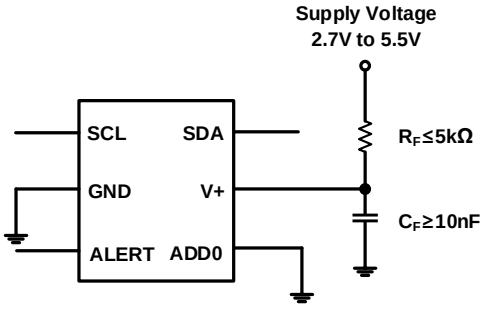


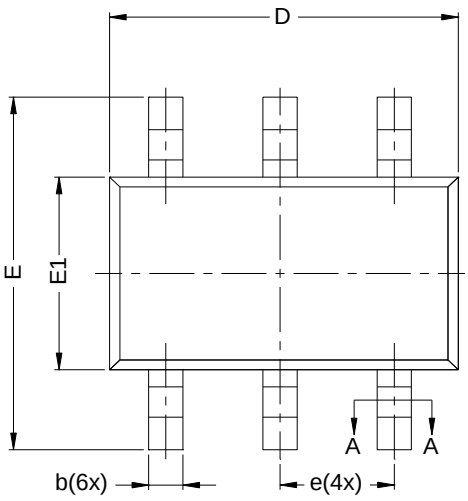
Figure 9. Noise Reduction Techniques

The GD30TS100N and GD30TS101N should be placed near the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

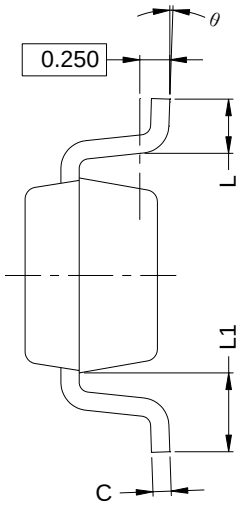
8 Package Information

8.1 Outline Dimensions

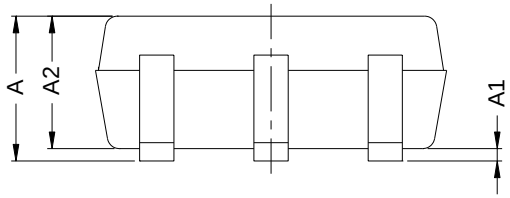
SOT23-6 Package Outline



TOP VIEW



SIDE VIEW



FRONT VIEW

NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the *Table 11. SOT23-6 dimensions(mm)*.

Table 11. SOT23-6 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0.00	0.05	0.10
A2	1.05	1.10	1.15
b	0.30	0.40	0.50
c	0.10	0.15	0.20
D	2.82	2.92	3.02
E	2.65	2.80	2.95
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.80	1.90	2.00
L	0.30	0.45	0.60
L1	0.60 REF		
θ	0°		8°

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30TS100NSSTR-I	SOT23-6	Green	Tape & Reel	3000	−55°C to +125°C
GD30TS101NSSTR-I	SOT23-6	Green	Tape & Reel	3000	−55°C to +125°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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